Claims:

1. A method of determining the timing for a synchronous integrated circuit, the circuit including a multiplicity of clocked elements interconnected by signal paths, the method comprising:

1) Forming predictions for timing delays in said signal paths in the integrated circuit;

2) Selecting a first such path, tracing wires in the integrated circuit forming the path (hereinafter referred to as victim wires) and determining adjacent and crossing wires thereto (hereinafter referred to as aggressor wires);

3) For each aggressor wire, determining the amount of perturbation coupling to the victim wires of the first path;

4) Dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;

5) Adding margins of error to the clocked timing of the victim wires independence upon the number of aggressor wires in one or more said categories.

2. A method according to claim 1, wherein step (3) is carried out taking into account one or more of the following factors:

a) whether the aggressor wire crosses or runs parallel to the victim wire;

b) the signal strengths in the victim and aggressor wires;

c) the layers in the integrated circuit which the wires are disposed;

d) operating conditions; and

e) the nature of aggressor wire

3. A method according to claim 1 or 2, wherein the aggressor wires are divided into three categories of likely, possible or unlikely to affect the timing of the victim wire.

4. A method according to claim 3, wherein the effect only of the likely category are taken into account.

5. A method according to claim 3, wherein the effect of the likely and possible categories are taken into account.

6. A method according to claim 3, wherein the effect of none of the categories is taken into account.

7. A method according to any of claims 3 to 6, wherein the effects of aggressor wires in any category are scaled according to their respective topological coupling and respective electrical signal coupling with the victim wire.

8. Apparatus for determining the timing of a synchronous integrated circuit, the circuit including a multiplicity of clocked elements interconnected by signal paths, the apparatus comprising:

1) Means for forming predictions for timing delays in said signal paths in the integrated circuit;

2) Means for selecting a first such path, tracing wires in the integrated circuit forming the path (hereinafter referred to as victim wires) and determining adjacent and crossing wires thereto (hereinafter referred to as aggressor wires);

3) Means for determining the amount of coupling, for each aggressor wire, to the victim wires of the first path;

4) Means for dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;

5) Means for adding margins of error to the clocked timing of the victim wires independence upon the number of aggressor wires in one or more of said categories.